REMARKS

This is in response to the office action mailed April 22, 2004.

Claims 1, 4, 6-14, 19 and 21-23 remain in the application. Claim 10 has been canceled.

Applicant has amended the claims to overcome the objections raised by the Examiner under 35 USC §112.

In digital receivers, the gain in the analog front end is typically set so that the entire dynamic range of an A to D converter is used. This enables better signal detection. Typically, once a signal is detected, the amplitudes can be monitored and used to provide a gain control signal. There is inherent in all circuitry a latency period. It takes some finite period of time for the signal received from a network, for example, to work its way through the circuitry to where it can be analyzed to determine its amplitude, before deciding whether the gain should be lowered or raised.

The present application attacks this problem of latency. As stated in the application on page 6:

> As will be seen the shift registers 32 and 41 record a history of whether the incoming signals are greater than the lower and upper thresholds. In effect, they provide a history in a trailing window of the past relative signal amplitudes. These, as will be seen, enable zero latency in starting the calculation of the AGC signal. For the embodiment of Figure 2, this history is stored as one bit data signals in the shift registers 32 and 41. Other memory means such as a random-access memory (RAM) can be used to store this information.

Importantly, these shift registers allow, in effect, a look back in time from when actual data signals were being received at the front end. The period of this looking back generally corresponds to the latency period. Thus, once a signal is

actually detected, the data is already there from which to calculate an AGC signal.

Claim 1 has been amended to make it clearer that the amplitudes being considered are a current relative amplitude, and an output from the shift register representing the relative amplitude of one of the samples taken at an earlier time. Similar language has been added to claim 23 to indicate that a current relative amplitude of sample and a relative amplitude of a sample taken earlier in time is used. Claim 19 has also been amended to make it clear that the prior amplitude from the tracked data was taken earlier in time. Consequently, all the independent claims now recite that the data from the shift registers or the tracked data was taken earlier in time, and is one way or another considered along with the current amplitude for controlling gain.

The claims were rejected under Halim, under §102, and under Halim and Sutterlin under §103.

Referring to the latching counter shown in Figure 3 of Halim, it includes a first counter and a second counter, both of which are being controlled by a signal representing the relative amplitude of an input signal. However, unlike the claims in the current application, there is no looking back in time before a signal is detected. Rather, Halim teaches simply living with the latency as follows (Col. 11, beginning at line 1):

> Next, the overall operation of the step AGC of the preferred embodiment should be considered. As noted hereinabove, the frequency of this clock signal on line 33 is 150 Hz. This gives it a period of 6.67 milliseconds. Consider for a moment the condition in which the input signal on line 11 undergoes a sudden precipitous drop in signal level such that the net result is that amplifier 12 needs to go from a state in which it is providing 0 dB of amplification to one which requires 18 dB of amplification. Under these

> circumstances counter 29 would begin counting sequential zeroes. It takes seven clock periods, or approximately 46.6 milliseconds for the seven consecutive zeroes to be counted. The first time this occurs, the signal adjustment controller 30 (FIG. 1) will cause the control signal in path 14 to step up the gain of amplifier 12 by 6 dB. Since under the described circumstances this is still inadequate, an additional 46.6 milliseconds is required for the next step, and yet another period of this magnitude for the third step to be achieved. Therefore, under the worst case condition, the attack time of the AGC is approximately 140 milliseconds.
>
> If the signal subsequently rises very rapidly, a similar analysis for the release time indicates that three sequential periods of 15 periods of the clock signal on line 33 must occur for the AGC to completely release returning amplifier 12 to its 0 dB amplification state. This leads to a release time on the order of 300 milliseconds.
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> Therefore, the present invention represents something of a tradeoff between speed of attack and release times of the AGC and use of the integrated circuit chip real estate for providing discrete level detectors.

Sutterlin is involved with providing the AGC control in conjunction with a snubbing or blanking circuit. This circuit prevents an input signal from being detected when there is noise on the line. More specifically, Sutterlin makes provisions to assure that the AGC signal is not affected by this blanking with the circuit shown in Figure 5.

Applicant submits that neither Halim or Sutterlin, alone or together, teach the present invention. There is no suggestion for gathering or storing information that can be used prior to signal detection for controlling an AGC signal.

Applicant submits that the claims are in condition for allowance, and an early allowance would be appreciated.

If there are any additional charges, please charge our Deposit Account No. 02-2666.

Respectfully submitted,
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